ABSTRACT

A semiconductor memory having a burst mode reading function in synchronization with a clock signal comprises a memory array composed of a plurality of memory cells, a sync read control circuit for releasing an upper group of the received address as a memory access address and a lower group of the received address as a burst address in synchronization with the clock signal, a sense amplifier for releasing an output data from each of the memory cells selected by the memory address, a decoder for decoding the burst address, a address latch for latching the decoded burst address in synchronization with the clock signal, a page selector for holding the output data and selecting corresponding one of the output data determined by the burst address of the address latch, and an output latch for latching the output data in synchronization with the clock signal.